WHAT IS CLAIMED IS:

1. A circuit operation verifying method for verifying that each of a number of circuit elements of a semiconductor circuit in layout design satisfies specifications, the method comprising the steps of:

loading condition information as electrical specifications on voltages and currents applied to the circuit elements, circuit diagram data representing connection information of the semiconductor circuit to be verified, and input patterns of voltages and currents used for circuit operation simulation with respect to time;

simulating operation of the semiconductor circuit to be verified while computing voltage values or current values with respect to time at the circuit elements of the semiconductor circuit to be verified based on the loaded circuit diagram data and input patterns and storing the computed values in a memory; and

verifying that the circuit elements of the semiconductor circuit to be verified satisfy the loaded condition information using the voltage values or the current values at the circuit elements stored in the memory.

2. The device of Claim 1, wherein the condition information includes electrical specifications representing current density values and heat generation amounts of the circuit elements;

the circuit diagram data of the semiconductor circuit to be verified includes layout information, and

current density analysis and heat generation analysis at positions inside the semiconductor circuit to be verified are performed based on the current values at the circuit elements and the layout information stored in the memory.

3. The method of Claim 1, wherein the condition information includes time specifications representing the frequency of violation against the electrical specifications or the time period for which a violation state is allowable, and

whether or not the frequency of violation or the violation allowable time period of each of the circuit elements of the semiconductor circuit to be verified satisfy the time specifications ~~is verified~~ using the voltage values or the current values with respect to time at the circuit element stored in the memory.

4. The method of Claim 1, wherein upon termination of the operation simulation and the condition verification of the semiconductor circuit to be verified, results of the condition verification are displayed on a waveform display apparatus displaying results of the operation simulation or a design apparatus used for circuit design or layout design of the semiconductor circuit.

5. The method of Claim 1, wherein a verification period during which the condition verification is to be executed for

the semiconductor circuit to be verified or a non-verification period during which no condition verification is to be executed is designated, and

the condition verification for the semiconductor circuit to be verified is executed during the verification period, or no condition verification for the semiconductor circuit to be verified is executed during the non-verification period.

6. The method of Claim 1, wherein the specifications in the condition information are commonly designated for all the circuit elements of the semiconductor circuit to be verified, or individually designated for the respective circuit elements.

7. The method of Claim 6, wherein low-precision, high-speed operation simulation is executed for the semiconductor circuit to be verified using the input patterns, to prepare operation information on the circuit elements of the semiconductor circuit to be verified and circuit hierarchical information on the semiconductor circuit to be verified,

thereafter, a plurality of circuit portions having the same operation pattern and the same hierarchical state in the semiconductor circuit to be verified are retrieved based on the operation information, the circuit hierarchical information, and the circuit diagram data, and

the specifications in the condition information are individually designated for only one circuit portion among the re-

trieved plurality of circuit portions so that the condition verification is executed for only circuit elements included in the one circuit portion.

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8. The method of Claim 1, wherein low-precision, high-speed operation simulation is executed for the semiconductor circuit to be verified using the input patterns, to prepare operation information on the circuit elements of the semiconductor circuit to be verified and circuit hierarchical information on the semiconductor circuit to be verified,

thereafter, a plurality of circuit portions having the same operation pattern and the same hierarchical state in the semiconductor circuit to be verified are retrieved based on the operation information, the circuit hierarchical information, and the loaded circuit diagram data, and

the retrieved plurality of circuit portions are united into one circuit portion, to reduce the circuit diagram data.

9. A circuit operation verifying apparatus for verifying that each of a number of circuit elements of a semiconductor circuit in layout design satisfies specifications, the apparatus comprising:

loading means for loading condition information as electrical specifications on voltages and currents applied to the circuit elements, circuit diagram data representing connection information of the semiconductor circuit to be verified, and input patterns of voltages and currents used for circuit op-

eration simulation with respect to time;

operation simulation means for simulating operation of the semiconductor circuit to be verified while computing voltage values or current values with respect to time at the circuit elements of the semiconductor circuit to be verified based on the circuit diagram data and the input patterns loaded by the loading means and storing the computed values in a memory; and

verification means for verifying that the circuit elements of the semiconductor circuit to be verified satisfy the specifications in the loaded condition information using the voltage values or the current values at the circuit elements stored in the memory.

10. The apparatus of Claim 9, further comprising:

waveform display means for displaying results of the operation simulation of the semiconductor circuit to be verified performed by the operation simulation means; and

design means used for circuit design or layout design of a semiconductor circuit,

wherein the results of the condition verification of the semiconductor circuit to be verified performed by the verification means are displayed on the waveform display means or the design means.